A HIGH PERFORMANCE TRANSCEIVER HYBRID IC FOR PHS HAND-SET OPERATING WITH SINGLE POSITIVE VOLTAGE SUPPLY

Masaaki Nishijima, Junji Itoh, Taketo Kunihisa, Takahiro Yokoyama, Shinji Yamamoto
Kazuo Miyatsuji, Mitsuru Nishitsuji and Osamu Ishikawa

Electronics Research Laboratory, Matsushita Electronics Corporation
3-1-1, Yagumo-nakamachi, Moriguchi, Osaka 570, Japan

ABSTRACT

A high performance transceiver hybrid IC(HIC) operating with single positive voltage supply has been developed for PHS hand-set. The HIC integrates a power amplifier(PA), a front-end(F/E) IC, a T/R SPDT switch(SW) and their peripheral circuits, which are mounted on the HIC circuit board with thick Cu metal heat-sink.

In the transmitter block, the PA with a SW exhibits with a low dissipation current of 190mA, a high power gain of 39.4dB and a low adjacent channel leakage power of -56.4dBc at an output power of 20.5dBm. In the receiver block, the F/E with a SW exhibits a low noise figure of 3.7dB, a low dissipation current of 4.8mA and a high conversion gain of 25.4dB. The HIC needs only single positive voltage supply of 3.5V. The HIC size is only 10mm×13mm×1.9mm.

INTRODUCTION

There are strong demands for a miniaturized and low power consumption IC which has a transceiver function and operates with single positive voltage supply in order to realize very compact and low-cost handy-phones. The RF circuits in the hand-sets usually need dual (positive and negative) voltage supply. Therefore, additional IC's and power sup ply for the IC's are necessary to generate the nega tive voltage. This negative voltage generation is one of the obstacles to realize very compact and low-cost handy-phones. Integration of the Transmitter/Receiver (T/R) section with a negative gate-bias voltage generator on a single chip(single chip IC) has been reported as one of the solutions which meet these demands[1]. However, the peripheral matching circuits lead to increase of circuit-board area occupied by this single chip IC.

This paper describes the development of a minia - turized and low power consumption transceiver HIC which operates with single positive voltage supply for 1.9GHz Japanese Personal Handy-phone System(PHS).

In order to realize the HIC mentioned above, the following three new technologies are developed.

*1)*MMIC chip set operating with single positive voltage supply,

*2)*Multi-chip Packaging by using a new plastic package,

*3)*HIC circuit-board having thick Cu backside-metal.

MMIC chip set

The PHS employs π/4 shift QPSK modulation, Time Division Multiple Access(TDMA) and Time Division Duplex(TDD) system. The PHS Hand-sets require an output power(Pout) of 19dBm and an adjacent channel leakage power(ACP) of less than -50dBc at antenna port.

A block diagram of the transceiver HIC for PHS is shown in Figure 1. This HIC is composed of three MMIC chips which are a PA MMIC, a F/E MMIC and a SW MMIC.

A. Power amplifier

The PA MMIC is a 3-stage amplifier. Three FET's and four matching cir cuits are integrated in the PA MMIC. A photograph of the MMIC chip is shown in Figure 2. The 1st, 2nd and 3rd FET's is fabricated by using pseudo morphic double heterojunction modulation doped MODFET(p-MODFET) process in order to realize low power consumption and single positive voltage operation[2]. The gate widths of the p-MODFET's is designed to be 0.2mm, 1mm and 4mm in order to achieve Pout more than 21dBm with low dissipation current, low ACP and high power gain.

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In the circuit design, the optimum source/load impedance's and the matching circuits are determined from the results of the source-pull/load-pull measurements and nonlinear simulation. Drain bias circuits are excluded to minimize the MMIC chip size[2]. As a result, the chip size becomes $1 \times 2mm^2$.

B. Front-end MMIC

The F/E MMIC is composed of an LNA, an LO amplifier(LOA) and a single-ended down converter mixer(MIXER). Intermediate tuned circuits and dual-gate GaAs MESFET's with self-biased common source are adopted for the F/E MMIC in order to realize low dissipation current, low noise figure and high image rejection without band-pass filter[3]. The bypass capacitors for the LNA, LO and MIXER and for the intermediate tuned circuits and input dc-cut out capacitors are integrated in the F/E MMIC by using high dielectric material of Barium Strontium Titanate(BST)[4]. The input matching circuits for the LNA and LOA are formed as external circuits. As a result, the chip size becomes $0.8 \times 1mm^2$. The MESFET's of the F/E MMIC are fabricated by using Ti/Al recessed gate and ion implantation process.

C. T/R SPDT switch

In order to handle the high power at 3.5V positive voltage, a feed-forward circuit configuration and the BST process are adopted for the SW MMIC[4]. The feed-forward circuit consists of a BST capacitor and a diode. BST Coupling capacitors are integrated in the SW MMIC. The chip size is $0.9 \times 1.05mm^2$. The MESFET's of the SW MMIC are fabricated by using the same process as the F/E MMIC. The SW MMIC features power for a 1dB compression of 30dBm, an insertion loss of 1.0dB and isolation over 25dB at a positive control voltage of 3.5V.

Multi-chip Packaging

Multi-chip packaging technology is important for stabilizing the characteristics of a PA, because it is sensitive to the thermal property of a package. We adopt a new 16pin plastic package with good thermal and electrical property. Photographs of the 16pin plastic package is shown in Figure 3. The lead-frame is exposed to its backside and acts as heat-sink. This package can provide low thermal resistance of 15°C/W(including thermal resistance of a PA MMIC chip and the lead-frame) and low ground inductance. A PA MMIC chip and a SW MMIC chip are simultaneously mounted on this package (PA+SW MMIC). A F/E MMIC chip is mounted on a mini-6pin plastic package.

HIC Circuit-board

Figures 4 and 5 show a schematic cross-sectional view and top view of the HIC, respectively. A packaged PA+SW MMIC and a packaged F/E MMIC are soldered on a HIC circuit-board (FR4) with all the peripheral matching components such as inductors, capacitors and resistors. The HIC circuit-board has thick Cu backside-metal with a thickness of 200μm that works as the heat-sink. The Cu backside-metal are electrically connected with the backside-metal of the 16pin plastic package through the via-holes. Therefore, there is no need to care about thermal problem on the main circuit-board of PHS hand-sets or cellular sets. The HIC has only four RF terminals(PA in, ANT, Lo in, IF out) and three bias terminals(PA Vdd, F/E Vdd, GND).The HIC size is only 10mm × 13mm×1.9mm.

HIC PERFORMANCE

A. Transmitter block

Figure 6 shows input-output power performance with the dissipation current(Idd), power gain, and adjacent channel leakage power(ACP) in the transmitter block of the PA with a SW. The PA with SW exhibits low dissipation current of 190mA, high power gain of 39.4dB and low adjacent channel leakage power of -56.4dBc at an output power of 20.5dBm and 3.5V single positive bias. Here, the idle current is 170mA, and the ACP is measured at -600kHz offset point apart from the center frequency of 1.9GHz for π/4 shift QPSK modulation signal.

B. Receiver block

Figure 7 shows the frequency response of noise figure(NF), conversion gain(CG) and image reduction ratio(IRR) in the receiver block of the F/E with a SW. A Low noise figure of 3.7dB, a high conversion gain of 25.4dB and a high image reduction ratio of 23.5dB are obtained at a RF

high conversion gain of 25.4dB and a high image reduction ratio of 23.5dB are obtained at a RF frequency of 1.9GHz and 3.5V single positive bias. Here, the IF frequency is 240MHz.

Figure 8 shows IF output power and third-order inter-modulation distortion as a function of the RF input power in the receiver block. A low Idd of 4.8mA are obtained at a RF input power of -40dBm and 3.5V single positive bias. The third-order output intercept point(IP3) is +6dBm.

CONCLUSION

We have demonstrated the high performance transceiver HIC operating with 3.5V single positive voltage supply for PHS hand-sets. The HIC integrates a PA, a F/E, a SW and their peripheral circuits, which are mounted on the HIC board with thick Cu metal heat-sink. The HIC size is only 10mm×13mm×1.9mm.

The transmitter block performance exhibits the low dissipation current of 190mA, the high power gain of 39.4dB and the low ACP of -56.4dBc at the Pout of 20.5dBm. The receiver block performance exhibits the low noise figure of 3.7dB, the low dissipation current of 4.8mA and the high conversion gain of 25.4dB. The newly developed HIC will contribute to the realization of very compact, low power consumption and low-cost PHS hand-sets.

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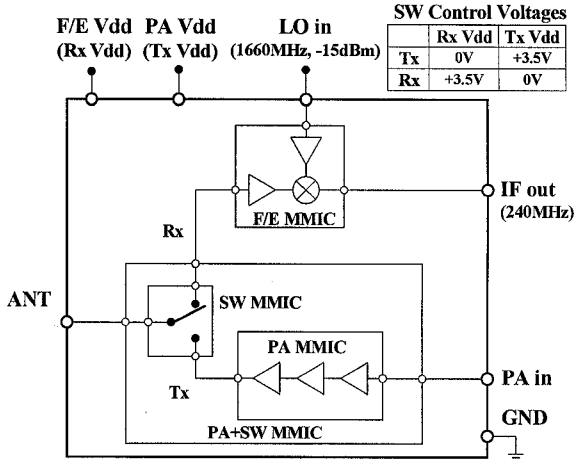

Fig.1 Block diagram of a transceiver HIC for PHS hand-sets. Tx Vdd:SW control voltage of the transmitter block-side. Rx Vdd:SW control voltage of the receiver block-side.

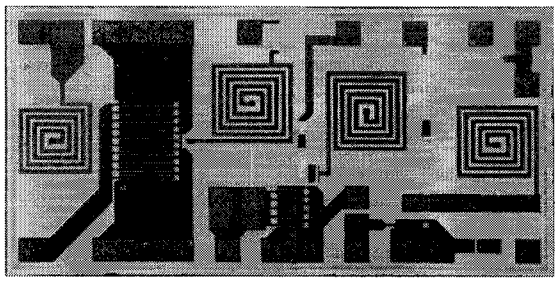

Fig.2 Photograph of the power amplifier MMIC chip. (chip size:1mm×2mm)

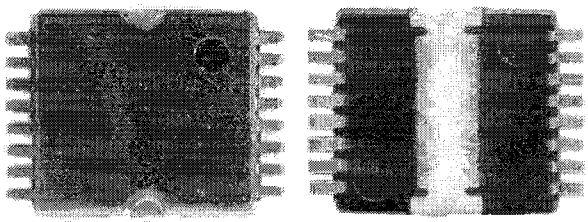

Fig.3 Photograph of the 16pin plastic package. (package size:6.2mm×4.6mm×1.1mm)

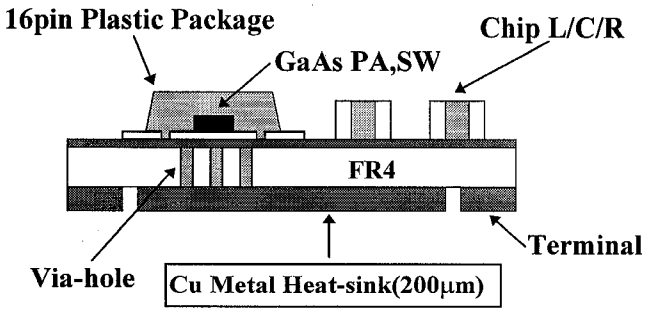

Fig.4 Schematic cross-sectional view of the HIC.

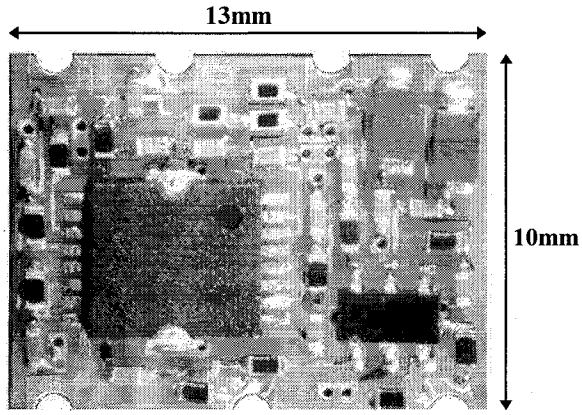

Fig.5 Top view of the HIC.
(HIC size: 10mm×13mm×1.9mm)

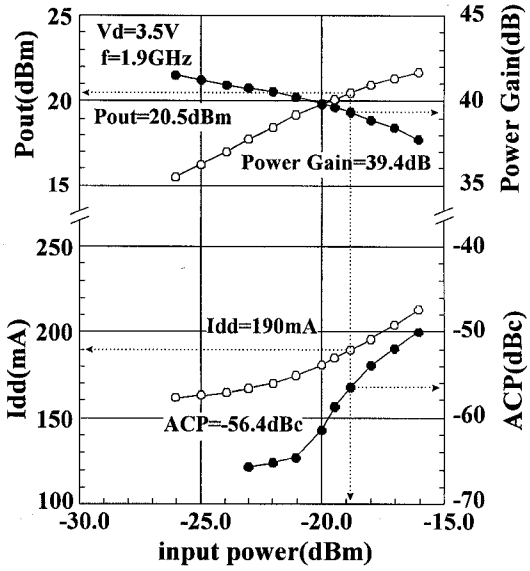

Fig.6 Transmitter block performance of the PA with SW as a function of input power for $\pi/4$ shift QPSK modulation signal.

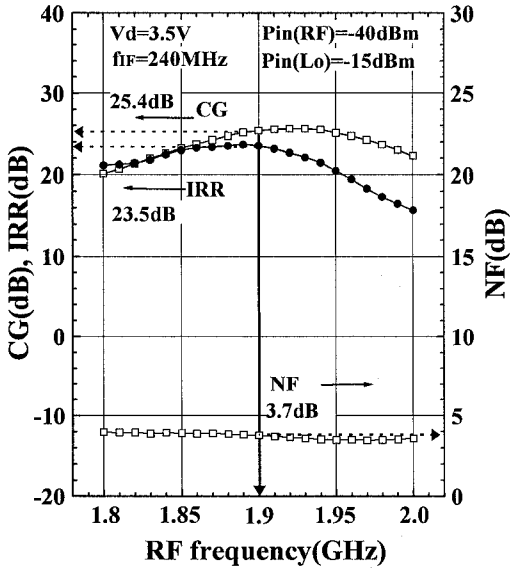

Fig.7 Receiver block performance of the F/E with SW as a function of RF frequency.
Pin(RF):RF input power.
Pin(Lo):Lo input power.

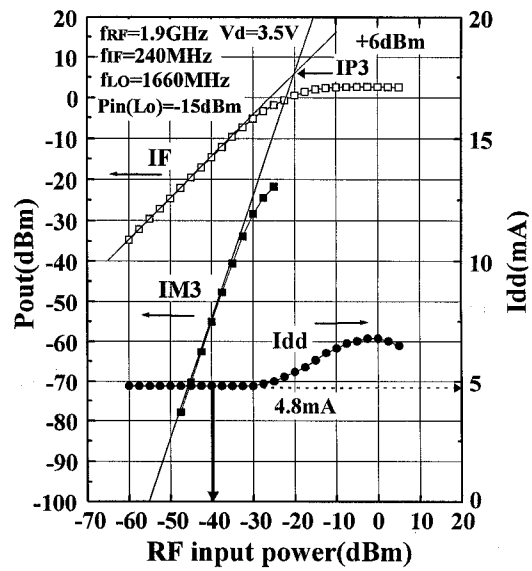

Fig.8 Receiver block performance of the F/E with SW as a function of RF input power.
Pin(Lo):Lo input power.